IDS - 09/30/2003

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)	Application / C nf. N .	Unknown 101 676, 929
	Filing Date	September 30, 2003
	First Named Invent r	Amit Singh
	Art Unit	~~Unknown~~ 2825
	Examiner Name	~~Unknown~~ TUYEN TO

Sheet	1	of	1	Attorney Docket Number	X-1495 US

OTHER – NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
TT		Donath, Wilm E.; "Placement and Average Interconnection Lengths of Computer Logic"; Circuits and Systems, IEEE Transactions on; Vol. 26, Issue 4; April 1979; pp. 272-277.	
TT		DeHon, Andre; "Balancing Interconnect and Computation in A Reconfigurable Computing Array'" International Symposium on Field Programmable Gate Arrays Archive Proeedings of the 1999 ACM/SIGDA Seventh International Symposium on FPGAs; 1999; pp. 69-78 [1-10].	
TT		Singh, Amit et al.; "Efficient Circuit Clustering for Area and Power Reduction in FPGAs"; International Symposium on FPGAs, 2002; Copyright Association for Computing Machinery; 8 pages.	
TT		Landman, B. S. et al.; "On a Pin Versus block Relationship for Partitions of Logic Graphs"; IEEE Transactions on Computers, Vol. C-20, No. 12, December 1971; pp. 1469-1479.	

Examiner Signature	[signature]	Date Considered	5/25/2006

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number. ² Applicant is to place a check mark here if English language Translation is attached.